UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/808,750	03/15/2001	Huy Thanh Vo	303.723US1	4340

21186 7590 07/16/2008
SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
MAI, SON LUU	

ART UNIT	PAPER NUMBER
2827	

MAIL DATE	DELIVERY MODE
07/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/808,750	VO, HUY THANH	
	Examiner	Art Unit	
	Son L. Mai	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13,15-41,45-53 and 55-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-41,45-53 and 55-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/02/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114 was filed in this application after a decision by the Board of Patent Appeals and Interferences, but before the filing of a Notice of Appeal to the Court of Appeals for the Federal Circuit or the commencement of a civil action. Since this application is eligible for continued examination under 37 CFR 1.114 and the fee set forth in 37 CFR 1.17(e) has been timely paid, the appeal has been withdrawn pursuant to 37 CFR 1.114 and prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 05/02/08 has been entered. Accordingly claims 1-13, 15-41, 45-53 and 55-57 are pending in the application.

Information Disclosure Statement

2. The information disclosure statement filed 05/02/08 has been considered.

Specification

3. Claim 1 is objected to because of the following informalities: "the strapping devices" in line 15 lacks antecedent basis. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-13, 15-41 and 45-48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As to claim 1, the recitation "wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline" and the recitation "wherein the strapping (line) strap a first half portion of a number of even wordlines in the memory array and a second half portion of a number of odd wordlines in the memory array" are contradictory. A strapping line cannot bypass only a portion in a middle region and first and second half portions in one embodiment.

Independent claims 5, 8, 15, 26, 30, 37 and 45 including similar language are rejected for being indefinite.

Claims 2-4, 6-7, 9-13, 16-18, 20-25, 31-36, 38-41 and 46-48 are rejected for depending on rejected claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-13 and 15-53, as best understood in view of the 112 rejection above, are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,940,315 issued to Cowles.

Regarding claim 1, Cowles discloses a memory array (figure 2A), comprising: a number of memory cells (see column 1, lines 28-38, Cowles teaches each cell has a gate region connected to a wordline, a drain connected to a bit line and a source connected to a capacitor) having a first source/drain region and a second source/drain region and a gate region; a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell; a number of wordlines (30-33) coupled to the gate region of at least one memory cell; a strapping line (112) of lower resistance than the wordlines coupled to a single continuous wordline (31) in a single array (memory bank 100) wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline, and wherein the strapping line is spaced apart from adjacent conductive structures by a distance greater than a wordline pitch (figure 2B shows that distance between strapping lines 112 and 113 is greater than a wordline pitch between wordlines 31 and 32), and wherein the strapping [lines] strap a first half portion of a number of even wordlines in the memory array and a second half portion of a number of odd wordlines in the memory array (straps 110 and 114 constitute a first half portion and strap 112 constitutes a second half portion); and at least two channels (such as node 150 in figure 2A) connecting the strapping line to a first and second end of the portion of the single wordline.

Regarding claim 2, Cowles also teaches that the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 3, Cowles also teaches the strapping line metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 4, Cowles teaches that the portion of the wordline bypassed by the strapping line comprises a first half of the memory cells coupled to the wordline (two middle memory arrays in figure 2A are considered as a first half of the memory cells).

Regarding claim 5, Cowles discloses a memory array (figures 2A, 2B) comprising: a number of memory cells (not shown. At column 1, lines 28-38, Cowles teaches each cell has a gate region connected to a wordline, a drain connected to a bit line and a source connected to a capacitor) having a first source/drain region and a second source/drain region and a gate region; a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell; a number of wordlines (30-33 in figure 2A) coupled to the gate region of at least one memory cell; a plurality of separate strapping lines (110-115) of lower resistance than the wordlines (column 4, lines 5-11) coupled to at least one of the number of wordlines (wordline 31) in a single array (memory block 100 in figure 2A) wherein the strapping lines bypass a plurality of separate portions of a single continuous wordline (column 3, lines 57-60), and wherein the strapping lines strap a first half portion of a number of even wordlines in the memory array and a second half portion of a number of odd wordlines in the memory array (straps 110 and 114 constitute a first half portion and strap 112 constitutes a second half portion); and a plurality of channels (at nodes such as node 150 in figure 2A) connecting the plurality of strapping layers to the wordline.

Regarding claim 6, Cowles also teaches that the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 7, Cowles also teaches the strapping line metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 8, Cowles discloses a memory device, comprising: a number of memory cells (not shown but inherent in a DRAM device) having a first source/drain region and a second source/drain region and a gate region, the memory cells forming a memory cell array; a number of source lines (not shown but inherent as lines connected to capacitors in a DRAM) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown but inherent as bit lines in a DRAM) coupled to the second source/drain region of at least one memory cell; a single array (arrays 20-23 in figure 2A are considered a single array for this rejection) of parallel wordlines (30-33) coupled to the gate region of at least one memory cell (as shown in figure 4 of the instant application), the array of parallel wordlines having a pitch (space between word lines 31 and 32 in figure 2B); a number of strapping devices (110 to 115 in figure 2A) which bypass portions of the wordlines in the single array of parallel wordlines, wherein at least one portion of a single continuous wordline is only in a middle region (strapping device 112) between a first and second end of the single continuous wordline, and wherein the strapping devices strap a first half portion of a number of even wordlines in the array and a second half portion of a number of odd wordlines in the array (straps 110 and 114 constitute a first half portion and strap 112 constitutes a second half portion), each strapping device (110-115) comprising: a strapping line of lower

resistance than the wordlines (column 4, lines 9-11), wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32); and at least two channels (at nodes such as node 150 in figure 2A) connecting each strapping line to a portion of a single wordline.

Regarding claim 9, Cowles teaches the memory device of claim 8 wherein the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 10, Cowles teaches the memory device of claim 9 wherein the metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 11, Cowles teaches the memory device of claim 8 wherein the portions of the wordlines in the array bypassed by the number of strapping devices comprises a plurality of end portions of the wordlines (figure 2A shows at nodes such as node 150 wordlines have a plurality of end portions).

Regarding claim 12, Cowles shows in figure 2A, the strapping devices (110 and 111) are located on alternating wordlines in the array.

Regarding claim 13, Cowles shows in figure 2A, the strapping devices (110, 112) are located on adjacent wordlines and staggered along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

Regarding claim 15, Cowles teaches an integrated circuit (figure 2A) comprising: at least one memory array (20-23) comprising: a number of memory cells (not shown but inherent in a DRAM device) having a first source/drain region and a second

source/drain region and a gate region; a number of source lines (not shown) coupled to the first source/drain region of at least one memory cell; a number of bit lines (not shown) coupled to the second source/drain region of at least one memory cell; a number of wordlines (30, 31 in figure 2A) in a single array (arrays 20-23 are considered as a single array) coupled to the gate region of at least one memory cell; a strapping line (112) of lower resistance than the wordlines (column 4, lines 9-11) coupled to a single continuous wordline (31) wherein the strapping line (112) bypasses only a portion of the wordline within the memory array in a middle region between a first and second end of the single continuous wordline, wherein the strapping line (112) is spaced apart from adjacent conductive structures (113 in figure 2B) by a distance greater than a wordline pitch (a space between 112 and 113 is greater than a space between 31 and 32), and wherein the strapping line bypasses a first half portion of a number of even wordlines in the memory array and bypasses a second half portion of a number of odd wordlines in the memory array (straps 110 and 114 constitute a first half portion and strap 112 constitutes a second half portion); at least two channels (at nodes such as node 150 in figure 2A) connecting the strapping line to a first and second end of the portion of the single continuous wordline (31); a row decoder (50 in figure 2A); a column decoder (40); and a sense amplifier (column 1, lines 35-38).

Regarding claim 16, Cowles teaches the integrated circuit of claim 15 wherein the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 17, Cowles teaches the integrated circuit of claim 16 wherein the metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 18, Cowles shows in figure 2A, the portion of the wordline bypassed by the strapping line (112) comprises a first half of the memory cells coupled to the wordline (a second half of the memory cells is in arrays 20 and 23).

Regarding claim 19, Cowles teaches an integrated circuit (figure 2A) comprising: at least one memory array (memory bank 100) comprising: a number of memory cells (not shown) having a first source/drain region and a second source/drain region and a gate region; a number of source lines coupled to the first source/drain region of at least one memory cell; a number of bit lines coupled to the second source/drain region of at least one memory cell; a single array of parallel wordlines (30-33) coupled to the gate region of at least one memory cell, the array of parallel wordlines having a pitch (space between word lines 31 and 32 in figure 2B); a number of separate strapping devices (110-115) which bypass separate portions of a single continuous wordline in the single array of parallel wordlines, and wherein the strapping devices strap a first half portion of a number of even wordlines in the memory array and a second half portion of a number of odd wordlines in the memory array (straps 110 and 114 constitute a first half portion and strap 112 constitutes a second half portion); and each strapping device (110-115) comprising: a strapping line of lower resistance than the wordlines (column 4, lines 5-11), wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113

being greater than the pitch between word lines 31 and 32); and at least two channels (at nodes such as node 150 in figure 2A) connecting the strapping line to the single continuous wordline (31); a row decoder (50); a column decoder (40); and a sense amplifier (column 1, lines 35-38).

Regarding claim 20, Cowles teaches the integrated circuit of claim 15 wherein the strapping line comprises metal (column 4, lines 5-11).

Regarding claim 21, Cowles teaches the integrated circuit of claim 16 wherein the metal comprises a refractory metal (tungsten and titanium are refractory metals; column 4, lines 5-11).

Regarding claim 22, Cowles shows in figure 2A, the integrated circuit of claim 19 wherein the portions of the wordlines in the array bypassed by the number of strapping devices comprises a plurality of end portions of the wordlines.

Regarding claim 23, Cowles shows in figure 2A, the strapping devices (110 and 111) are located on alternating wordlines in the array.

Regarding claim 24, Cowles shows in figure 2A, the strapping devices (110, 112) are located on adjacent wordlines and staggered along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

Regarding claim 25, Cowles shows in figure 2A, the strapping devices (110 to 115) strap a first half portion (arrays 21 and 22) of a number of even wordlines in the array and a second half portion (arrays 20 and 23) of a number of odd wordlines.

Regarding claims 26-29, Cowles shows in figure 3, information handling device comprising: a processing unit (334); at least one memory array (348). The limitations of the memory array are discussed in claims 15-18.

Regarding claims 30-36, Cowles teaches information handling device (figure 3) comprising: a processing unit (344); at least one memory array (348). The limitations of the at least one memory array are discussed in claims 19-25.

Regarding claim 37, Cowles discloses a method of reducing a wordline RC time constant (to minimize signal delays; column 1, lines 57-64) comprising: spacing a number of strapping devices (110-115 in figure 2A) over wordlines (30-33) within a single memory array (memory bank 100) apart from adjacent strapping devices by a distance greater than a wordline pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32), wherein the strapping devices bypass a first half portion of a number of even wordlines in the memory array and bypass a second half portion of a number of odd wordlines in the memory array (straps 110 and 114 constitute a first half portion and strap 112 constitutes a second half portion); and connecting individual strapping devices (112 and 113) to portions in a middle region between a first and second end of single continuous wordlines (31 and 33) using at least two channels (at nodes 150) for each strapping device; activating a first number of transistors (transistors of memory cells connected to word line 31 in regions 21 and 22) coupled to a first portion of a wordline; and activating a second number of transistors (transistors of memory cells connected to the word line 31 in regions 20 and 23) coupled to a second portion of a wordline, wherein a signal

used for activating the second number of transistors bypasses the first portion of the wordline through a strapping device of lower resistance than the first portion of the wordline (column 4, lines 12-19); activating a selected bitline in the memory array associated with a selected memory cell (column 1, lines 32-38); discharging the selected memory cell through a selected transistor, the selected transistor being activated by both the selected row and the selected bitline (column 1, lines 32-38); and sensing the presence or absence of a charge from the selected memory cell through the use of a sense amplifier (column 1, lines 32-38).

Regarding claim 38, Cowles discloses that activating a second number of transistors (transistors of memory cells connected to the word line 31 in regions 20 and 23 in figure 2A) coupled to a second portion of a wordline comprises: sending a signal through a first channel to a metal strapping line (thru node 150 in figure 2A); sending the signal through the metal strapping line (112); and sending the signal through a second channel (at the other end of line 112) to the second portion of the wordline.

Regarding claim 39, Cowles teaches that sending the signal through the metal strapping line (112 in figure 2A) comprises sending the signal through a refractory metal strapping line (titanium and tungsten are refractory metals; column 4, lines 5-11).

Regarding claim 40, Cowles shows in figure 2A, activating a first number of transistors coupled to a first portion of a wordline (transistors of memory cells connected to the word line 31 in regions 21 and 22) comprises activating a first number of transistors coupled to a first half of the wordline.

Regarding claim 41, Cowles shows in figure 2A, activating a selected row (word line 31) in a memory array comprises bypassing multiple portions (in regions 21 and 22) of the wordline using multiple strapping devices (strapping line 112 has 1 portion in region 21 and a portion in region 22) of lower resistance than the wordline (column 4, lines 9-11).

Regarding claim 45, Cowles teaches a method of forming a memory device (figures 2A and 2B) comprising: forming a number of memory cells (not shown but understood as inherent in a semiconductor memory device; column 3, lines 22-33) having a first source/drain region and a second source/drain region and a gate region (such as a memory cell shown in figure 4 of the instant application), the memory cells forming a memory cell array (figure 2A); coupling a number of source lines to the first source/drain region of at least one memory cell (source terminals of transistors in figure 4 of the instant application are connected to a source line); coupling a number of bit lines to the second source/drain region of at least one memory cell (drain terminals of the transistors are connected to bit lines); attaching a number of wordlines to the gate region of at least one memory cell to form a single array (gate terminals of the transistors are connected to word lines); attaching a strapping line (112 in figure 2A) of lower resistance than the wordlines (column 4, lines 9-11) to a single continuous wordline (31 in figure 2A) wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline, wherein the strapping line (112) is spaced apart from adjacent conductive structures (113) by a spacing greater than a wordline pitch (figure 2B shows a distance between strapping

lines 112 and 113 being greater than the pitch between word lines 31 and 32) and wherein the strapping line bypasses a first half portion of a number of even wordlines in the memory array and bypasses a second half portion of a number of odd wordlines in the memory array (straps 110 and 114 constitute a first half portion and strap 112 constitutes a second half portion); and connecting the strapping line (112) to the single wordline (31) by forming at least two channels (at nodes such as 150) from the strapping line to the single continuous wordline.

Regarding claim 46, Cowles discloses that attaching at least one strapping line (112) of lower resistance than the wordlines (column 4, line 9-11) to at least one of the number of wordlines comprises attaching at least one metal strapping line.

Regarding claim 47, Cowles teaches that attaching at least one metal strapping line (112) comprises attaching at least one refractory metal strapping line (titanium and tungsten are refractory metals; column 4, lines 5-11).

Regarding claim 48, Cowles discloses that attaching at least one strapping line (112) of lower resistance than the wordlines to at least one (31) of the number of wordlines comprises attaching multiple strapping lines (strapping line 112 has at least two portions: one in region 21 and one in region 22) to bypass multiple portions of a single wordline.

Regarding claim 49, Cowles teaches a method of forming a memory device (figure 2A) comprising: forming a number of memory cells (not shown but understood as inherent in a semiconductor memory device; column 3, lines 22-33) having a first source/drain region and a second source/drain region and a gate region (such as a

memory cell shown in figure 4 of the instant application), the memory cells forming a memory cell array (figure 2A); coupling a number of source lines coupled to the first source/drain region of at least one memory cell (source terminals of transistors in figure 4 of the instant application are connected to a source line); coupling a number of bit lines coupled to the second source/drain region of at least one memory cell (drain terminals of the transistors are connected to bit lines); attaching a single array of parallel wordlines (30-33 in figure 2A) to the gate region of at least one memory cell, the single array of parallel wordlines having a pitch (a space between word lines 31 and 32 in figure 2B); attaching a number of strapping lines (110-115) of lower resistance than the wordlines (column 4, lines 9-11) which bypass portions of the wordlines in the array of parallel wordlines and wherein the strapping lines are attached on a first half portion of a number of even wordlines in the memory array and attached on a second half portion of a number of odd wordlines in the memory array (straps 110 and 114 constitute a first half portion and strap 112 constitutes a second half portion); and, wherein at least one portion of a single continuous wordline (31) is only in a middle region between a first and second end of the single continuous wordline, wherein the strapping lines are each located a distance from each other that is greater than the pitch (figure 2B shows a distance between strapping lines 112 and 113 being greater than the pitch between word lines 31 and 32), and wherein adjacent strapping lines (110 and 112) bypass different portions of adjacent wordlines within the memory cell array; and connecting the strapping lines (112) to the wordlines by forming at least two channels (at nodes such as node 150) from each strapping line to individual wordlines.

Regarding claim 50, Cowles teaches that attaching a number of strapping lines (112, 113) comprises attaching a number of metal strapping lines (column 4, line 9-11).

Regarding claim 51,Cowles teaches that attaching a number of metal strapping lines comprises attaching a number of refractory metal strapping lines (titanium and tungsten are refractory metals; column 4, lines 5-11).

Regarding claim 52, Cowles teaches that attaching a number of strapping lines (110 and 112) comprises attaching the strapping lines on alternating wordlines (30 and 31) in the array.

Regarding claim 53, Cowles teaches that attaching the strapping lines comprises attaching the strapping lines (110, 112) on adjacent wordlines (30, 31) and staggering the strapping lines along the wordlines such that the portions of the adjacent wordlines that are bypassed are not adjacent to each other.

7. Claims 55-57 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,708,621 issued to Tanoi.

Regarding claim 55, Tanoi teaches a memory device comprising: a memory array (106 in figure 16) including a number of memory cells (6 in figure 1); an even row decoder (connected to driver 31) located on a first side (right side) of the memory array; an odd row decoder (connected to driver 30) located on a second side (left side) of the memory array; a single column decoder (YDEC 16 in figure 1) connected to the memory array; a number of parallel wordlines (figure 16) local to the memory array coupled to gate regions of memory cells, including one or more even wordlines (120) coupled to

the even row decoder, and one or more odd wordlines (110) coupled to the odd row decoder, the odd wordlines arranged alternately with the even wordlines; and a number of strapping lines (108, 118) having lower resistance than the wordlines (see column 9, lines 33-35) and connected to bypass portions of the wordlines within the memory array, wherein a strapping line (108) connected to an odd wordline (110) bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder, wherein a strapping line (118) connected to an even wordline (120) bypasses only a portion of the even wordline within the memory array nearer the even row decoder.

Regarding claim 56, Tanoi teaches that the even row decoder (connected to driver 31) is located directly adjacent the first side (right side) and the odd row decoder (connected to driver 30) is located directly adjacent the second side (left side).

Regarding claim 57, Tanoi teaches a strapping line (108 in figure 16) connected to an odd wordline (110) bypasses only one half of the wordline (from plug 112 to plug 116) within the memory array nearer the odd row decoder (connected to driver 30) and a strapping line (118) connected to an even wordline (120) bypasses only one half of the wordline (from plug 122 to plug 126) within the memory array nearer the even row decoder (connected to driver 31).

Conclusion

8. The prior art made of record is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on M-F from 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

07/11/08

/Son L. Mai/
Primary Examiner, Art Unit 2827